Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examination – June – 2017**

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| **Code :** | **14EC2072** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ANALYSIS AND DESIGN OF DIGITAL IC** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | Indicate the OUT value in Fig 1 when IN-1, IN-2, IN-3 is 1,1,0 respectively. | CO1 | 2 |
| b. | Justify the statement “NMOS transistors pass strong zero but not strong one”. | CO3 | 4 |
|  | c. | Obtain the voltage transfer curve of CMOS inverter, analyze it and indicate the status of PMOS and NMOS transistors in different regions and also discuss voltage and current parameters in these regions. | CO2 | 14 |
| (OR) | | | | |
| 2. | a. | Distinguish between linear and saturation operating modes of NMOS transistors with respect to its output current. | CO2 | 4 |
| b. | Give the lumped representation of the MOSFET capacitances. | CO2 | 2 |
| c. | With neat diagram and equation explain different regions of operation of NMOS transistor. Obtain the characteristic curve for the same. | CO2 | 14 |
| 3. | a. | Justify with diagram the need for a level restorer circuit in pass transistor logic. | CO2 | 3 |
|  | b. | Draw the block diagram of domino logic design style. | CO1 | 3 |
|  | c. | Analyze and illustrate the different types of power dissipation that occurs in CMOS inverter design with mathematical equations. | CO2 | 14 |
| (OR) | | | | |
| 4. | a. | Design 2:1 MUX using transmission gate and justify the same. | CO1 | 4 |
|  | b. | Compare the static power consumption of complementary CMOS and ratioed logic design styles. | CO3 | 3 |
|  | c. | Mention the advantage of transmission gate logic as compared to pass transistor logic. | CO3 | 3 |
|  | d. | With timing diagram, illustrate the problem associated with cascading dynamic gates and provide a solution for the same. | CO2 | 10 |
| 5. | a. | Give the relation between fall time and rise time for equally sized n and p transistors in an inverter. | CO2 | 2 |
|  | b. | Implement F=A + BCD using complementary CMOS logic design style. | CO1 | 4 |
|  | c. | With schematic and timing diagram cascade dynamic gates, analyze the behaviour and provide the solution for the same. | CO2 | 14 |
| (OR) | | | | |
| 6. | a. | Differentiate between Analytical delay model and Empirical Delay model. | CO2 | 4 |
|  | b. | Design F = ((AB)+(CD)) using domino logic design style and explain its operation. | CO1 | 16 |
| 7. | a. | List the parameters required to fix the maximum clock frequency for sequential logic circuits. | CO1 | 2 |
|  | b. | With example, differentiate between foreground and background memory. | CO3 | 2 |
|  | c. | Design and explain the operation of dynamic transmission gate edge triggered registers | CO1 | 8 |
|  | d. | Analyze the impact of clock overlap in master slave register and provide a solution for the same with neat diagram. | CO2 | 8 |
| (OR) | | | | |
| 8. | a. | Justify the statement that dynamic memories stores data for a short period of time. | CO3 | 2 |
|  | b. | With timing diagram explain positive latch. | CO1 | 2 |
|  | c. | Mention the need for designing a low voltage static latch. Discuss the challenges in the design and provide a solution for the same in the design. | CO3 | 8 |
|  | d. | Illustrate the clock overload issue in master slave register design and mention the challenges faced in providing the solution for the same. | CO3 | 8 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Design a positive edge triggered master slave register that is insensitive to clock overlap and explain its operation. | CO1 | 10 |
|  | b. | Design a pipelined datapath for the computation of log(la+bl) and explain its operation by comparing it with the conventional design. | CO1 | 10 |

ALL THE BEST